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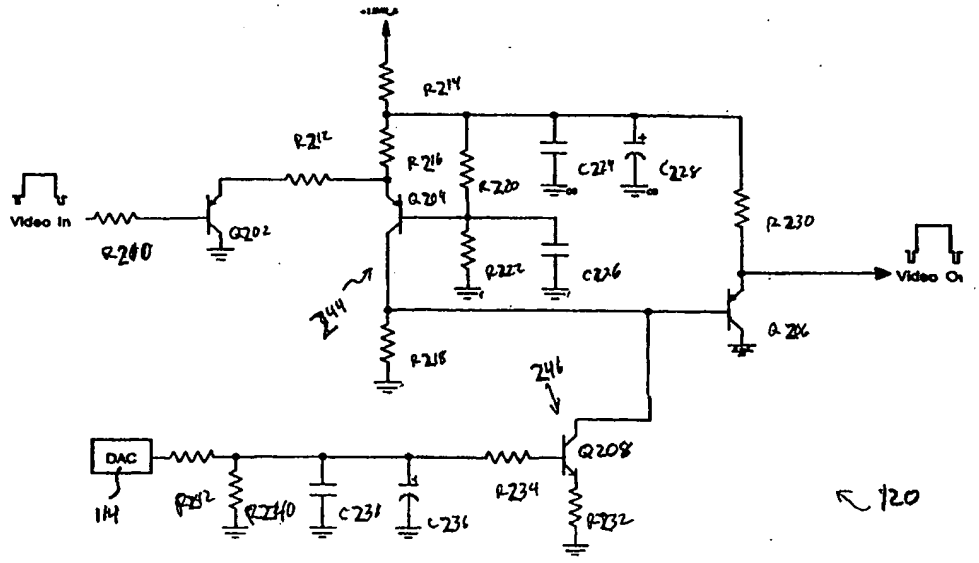

(57) Abstract

A method and apparatus within a television receiver for electronically aligning signals within the receiver by controlling support circuitry for an IF module. A video amplifier is coupled to an output of the IF module. A control voltage source (DAC 114) controls a DC level control circuit within the video amplifier (244) such that the video signal is amplified and DC level shifted to align the video signal with down stream circuitry.

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VIDEO AMPLIFIER WITH INTEGRATED DC LEVEL SHIFTING

This application claims the benefit of U.S. provisional application serial no. 60/102,429 filed September 30, 1998, which is hereby incorporated herein by reference.

BACKGROUND OF THE DISCLOSURE

1. Field of the Invention

The invention relates to television receivers and, more particularly, the invention relates to a video amplifier for a television receiver.

BACKGROUND OF THE INVENTION

In modern television receivers, a microprocessor provides command and control information through an I^2C bus interface to provide various control functions. The I^2C bus is coupled to a module (an IF integrated circuit) comprising a tuner, IF, and stereo decoder. To achieve the best picture and sound performance, the microprocessor may control 8 or more alignment functions and various switch functions through the I^2C bus interface. These functions provide factory alignment of various signal characteristics such as video output amplitude and dc-level, RF AGC delay threshold, and the like. Such electronic alignment is performed to ensure that a consistent picture quality between televisions occurs in retail show rooms; to ensure that consistent picture equality results between inputs of a television with multiple tuners or multiple auxiliary inputs; and to maintain signal levels within dynamic range limitations of the receiver circuitry.

One aspect of electronic signal alignment control that is not presently addressed in the art is the ability to control the DC level of a video signal that is produced by an IF integrated circuit. Such a signal alignment feature enables the IF integrated circuit to be matched to down

stream circuits such that the IF integrated circuit can be used in a greater number of television receivers.

Therefore, there is a need in the television receiver art for an economical solution that enables a system microprocessor to control the DC level of a video signal.

SUMMARY OF THE INVENTION

The present invention is a method and apparatus within a television receiver for electronically aligning signals within the receiver by controlling the DC level of a video signal. The television receiver comprises a IF integrated circuit that provides a tuner, IF and stereo decoder. The invention uses a digital-to-analog converter (DAC) integrated circuit to control a DC level produced by a video amplifier that is coupled to the output of the IF integrated circuit. In one embodiment of the invention, a system microprocessor is coupled through an I^2C bus to a DAC that controls the video amplifier. The video amplifier comprises a DC video level circuit that applies a DC level to the amplified video signal. Additionally, the video amplifier is a non-inverting amplifier such that the output of the IF integrated circuit is polarity matched to downstream circuitry.

BRIEF DESCRIPTION OF THE DRAWINGS

The teachings of the present invention can be readily understood by considering the following detailed description in conjunction with the accompanying drawings, in which:

FIG. 1 depicts a portion of a television receiver that is arranged in accordance with the present invention;

FIG. 2 is a schematic diagram of a non-inverting video amplifier with DC level control; and

FIG. 3 is a graph of the video output sync-tip Dc level versus the register value of the DAC produced by the video amplifier of FIG. 2.

To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures.

DETAILED DESCRIPTION

FIG. 1 depicts a block diagram of a portion 100 of a television receiver comprising a signal processing module 106 as well as components of the present invention that support the operation of the module 106. The module 106 is known as an IF integrated circuit that performs video signal processing upon a television signal to produce a baseband video signal. The baseband video signal is amplified by a video amplifier 120 in accordance with the present invention. Specifically, the video amplifier 120 contains DC level shifting circuit that enables the DC level of the output video signal to be controlled by a system microprocessor 158 such that the video signal can be electronically aligned.

More specifically, the signal processing module 106 is, for example, a model LA7577N IF integrated circuit manufactured by Sanyo Corporation. The module 106 comprises an IF circuitry for both sound (SIF) and picture (PIF). The audio circuitry portion 154 of the module 106 comprises an SIF amplifier 146 and SIF AGC 148, down converter 147 (mixer), a limiting amplifier 150 and an FM detector 152. Supporting the audio circuitry 154 is a 4.5 MHz bandpass filter 108. The audio circuitry 154, although it is a part of the television receiver module 106, forms no part of the present invention.

The video portion 156 of the module 106 comprises a PIF amplifier 134, a video detector 132, a phase detector 130, a voltage controlled oscillator 140, an internal video amplifier 138, an equalization amplifier 144, a Nyquist slope canceller 142, an APC switch 128, a lock detector 124, and IF AGC circuit 126 and an RF AGC amplifier 122. Supporting the video portion 156 of the module 106 is a PIF saw filter 102, a phase lock loop filter 104, a PIF AGC

filter 118 and an external video amplifier 120 at the output of the module 106, as well as a sound trap 110 and a video level circuit 112. The IF video input is coupled to the PIF SAW filter 102 that filters the video signal. The SAW filtered video is amplified in IF amplifier 134, then down converted to baseband using the video detector 132. The video detector 132 is driven by the voltage controlled oscillator (VCO) 140. The baseband video is amplified by internal video amplifier 138. The amplified signal is filtered by the sound trap 110 and applied to the input of the video level control circuit 112. The operation of the video level circuit affects the IF AGC 126 which in affects the gain of the PIF amplifier 134 and, thus, the video signal amplitude. The output of the video level control circuit 112 is applied to the equalization amplifier 144 to control the amplitude of the video signal. The output of the equalization amplifier 144 is further amplified by video amplifier 120 to form the video output signal. The output of the PIF AGC filter is coupled to the lock detector 124 that drives the APC switch 128. The APC switch 128 selects the mode of operation for the PLL loop filter, i.e., whether the filter is operated in broad band mode (used during signal acquisition) or narrow band mode (used after PLL lock). The system microprocessor 158 couples digital control signals to a plurality of DACs 114 (e.g., eight DACs in a single integrated circuit package such as a TDA8444 manufactured by Philips Corporation) that, in turn, control the operation of various aspects of the IF module 106 and, in particular, control the level circuit 112, the PIF mute 116, and the video amplifier 120.

It is important to note that the video level circuit within the IF AGC loop and the IF amplifier gain is set by detecting the sync-tip level. As such, a change in the DC level of the video signal, as performed by the level circuit 112, changes the sync-tip level and the IF AGC loop gain. Consequently, a change in DC level by the level circuit 112 controls the amplitude of the video signal. A detailed discussion of the level circuit 112 and the PIF

mute circuit appears in PCT patent application number _____, filed simultaneously herewith, (Attorney Docket Number 89203) and incorporated herein by reference.

The specific interconnections shown in FIG. 1 are representative of the interconnections within the LA7577N module 106. Those skilled in the art will realize that the inventive use of the video amplifier 120 described in detail below could be used in many other video processing applications.

FIG. 2 depicts a schematic diagram of a non-inverting video amplifier 120 in accordance with the present invention. The video input signal is produced at the output pin 21 of the IF integrated circuit such as the LA7577 shown in FIG. 1. The video amplifier 120 is employed as the external video amplifier connected to the video output terminal of the IF integrated circuit. This amplifier provides both video signal amplification and DC level shifting of the amplified video signal.

The video signal is applied to resistor R210 that couples the signal to transistor Q202 (input buffer) Transistor Q206 forms an output buffer for the video amplifier 120. Resistor R214 capacitor C228, and capacitor C224 are used to filter the power supply voltage. Resistor R220 and resistor R222 set the base of transistor Q204 to a constant voltage above the maximum video input signal level. The amplifier voltage gain of the common base amplifier 244 (comprising transistor Q204, resistor R216, resistor R212, resistor R218, resistor R220, resistor R222 and capacitor C226) is equal to the ratio of R218/R212. The DC level of the video output signal is determined by the DC current through resistor R218, which is adjusted by stealing current with the constant current source of transistor Q208. The control voltage from a DAC 114 is attenuated and filtered by resistor R242 and R240, and capacitors C238 and C236. The filtered control signal is coupled to the amplifier 244 through a current source 246 comprising transistor Q208 and resistors R234 and R232.

In operation, as the DAC output voltage increases, transistor Q208 collector current increases, the DC current through R218 decreases and thus the video output DC level decreases. The relationship 300 between the output DC voltage of the video amplifier in response to the DAC output voltage is depicted in FIG. 3, where the horizontal axis 302 is control voltage (DAC values) and the vertical axis 304 is the sync tip level voltage level (video DC level).

By way of example, the video input sync tip level production spread is 3.01 to 4.15 VDC, while the video output requirement is 2.5 ± 0.5 VDC. The DC level adjustment was designed to set the video output sync tip level to 2.5 ± 0.1 VDC. The desired amplifier gain was 1.65 which was achieved by setting R218 and R222 to 3300 and 2000 ohms, respectively.

The ratio of R220/R222 is set to equal the ratio of R222/R212 to optimize the power supply ripple rejection. If the two ratios are equal, the output is not affected by relatively small changes in the power supply voltage. This is important because the low pass filter formed by R214, C224 and C228 have little to no effect at very low frequencies. Although the output buffer Q206 is shown as an PNP transistor and NPN transistor could also be used. Lastly, C226 can be used to provide additional noise filtering and/or compensate for Q204 junction capacitance to improve the video bandwidth of the circuit.

The present invention provides circuitry that facilitates television receiver signal alignment using a system microprocessor to control the signal alignment operation through the system I^2C bus. The circuitry includes a non-inverting video amplifier having a controlled DC level. As such, the inventive circuitry provides additional signal alignment functionality during factory alignment and testing through the television receiver system's existing microprocessor and I^2C bus. The video amplifier amplifies in a non-inverting manner such that the output of the IF integrated circuit module, after

amplification and level shifting, remains compatible with down stream circuitry that expects a certain polarity video signal.

Although various embodiments which incorporate the teachings of the present invention have been shown and described in detail herein, those skilled in the art can readily devise many other varied embodiments that still incorporate these teachings.

What is claimed is:

1. A video amplifier comprising:
an input buffer;
an amplifier coupled to said input buffer;
an output buffer coupled to said video amplifier; and
a DC level control circuit coupled to said video amplifier.

2. The apparatus of claim 1 wherein said amplifier further comprises:
a transistor connected in a common-base configuration.

3. The apparatus of claim 1 wherein said amplifier is a non-inverting amplifier.

4. The apparatus of claim 1 wherein said DC level control circuit comprises:
a current source that controls a current through said amplifier in response to said control signal.

5. The apparatus of claim 2 wherein said transistor has a base that is connected to ground through a capacitor.

6. The apparatus of claim 2 wherein said transistor has a collector coupled through a first resistor to said input buffer amplifier and an emitter coupled through a second resistor to ground, where a first ratio of a value of said second resistor to a value of said first resistor establishes the amplifier gain.

7. The apparatus of claim 2 wherein said transistor has a base and a third resistor coupled from said base to a power supply and a fourth resistor coupled from said base to ground, where a second ratio of said third resistor to said fourth resistor is equal to said first ratio.

8. Apparatus for aligning signals in a television receiver comprising:

an IF integrated circuit for processing a television signal and producing a video signal;

a non-inverting video amplifier, coupled to said IF integrated circuit to amplify said video signal;

a controller, coupled to said non-inverting video amplifier, for controlling a DC level of said amplified video signal.

9. The apparatus of claim 8 wherein said controller comprises:

a microprocessor;

a digital-to-analog converter; and

a bus coupling said microprocessor to said digital-to-analog converter.

10. The apparatus of claim 8 wherein said non-inverting video amplifier further comprises:

an input buffer;

an amplifier coupled to said input buffer;

an output buffer coupled to said amplifier; and

a DC level control circuit coupled to said amplifier.

11. The apparatus of claim 10 wherein said amplifier further comprises:

a transistor connected in a common-base configuration.

12. The apparatus of claim 10 wherein said DC level control circuit comprises:

a current source that controls a current through said amplifier in response to said control signal.

13. The apparatus of claim 11 wherein said transistor has a base that is connected to ground through a capacitor.

14. The apparatus of claim 11 wherein said transistor has a collector coupled through a first resistor to said input

buffer amplifier and an emitter coupled through a second resistor to ground, where a first ratio of a value of said second resistor to a value of said first resistor establishes the amplifier gain.

15. The apparatus of claim 11 wherein said transistor has a base and a third resistor coupled from said base to a power supply and a fourth resistor coupled from said base to ground, where a second ratio of said third resistor to said fourth resistor is equal to said first ratio.

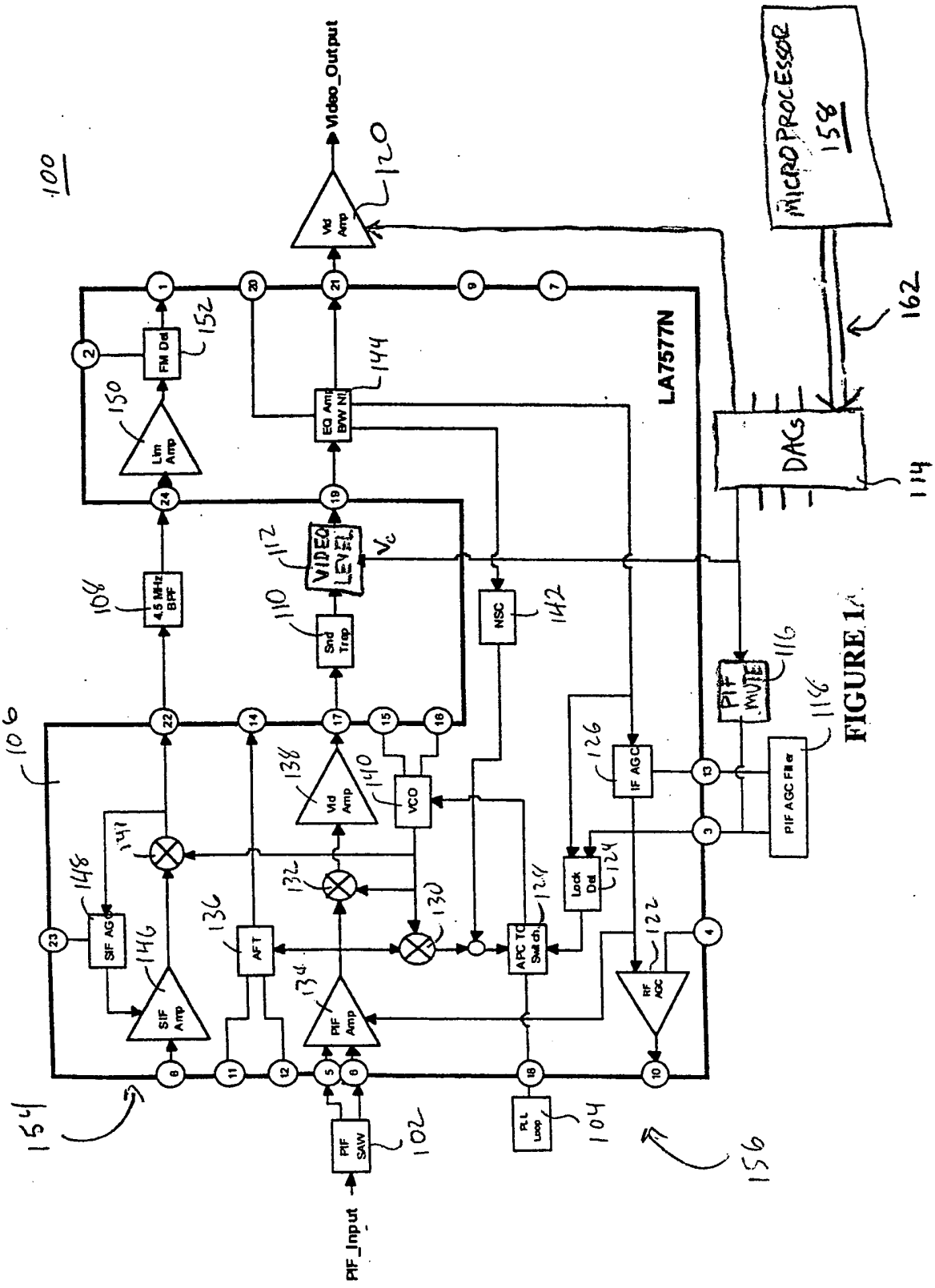
16. A method of aligning a signal in a television receiver comprising the steps of:

providing a video signal from an IF integrated circuit;

generating a control signal for a video amplifier that is coupled to the output of said IF integrated circuit;

coupling the control signal to a DC level shifting circuit in said video amplifier;

amplifying said video signal and shifting a DC level of said amplified video signal in response to the control signal.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Video_Output
120
Vid Amp
MICRO PROCESSOR
158
162
LA7577N
DACs
114
FM Det
152
150
Lim Amp
144
EQ Amp BW NI
VIDEO LEVEL
112
Vc
108
4.5 MHz BPF
110
Snd Trap
NSC
142
PIF MUTE
116
106
138
Vid Amp
140
VCO
126
IF AGC
PIF AGC Filter
118
141
148
SIF AGC
146
SIF Amp
136
AFT
132
130
134
PIF Amp
APC TC Switch
128
Lock Det
124
122
RF AGC
154
PIF SAW
102
PLL Loop
104
156
PIF_Input

FIGURE 1

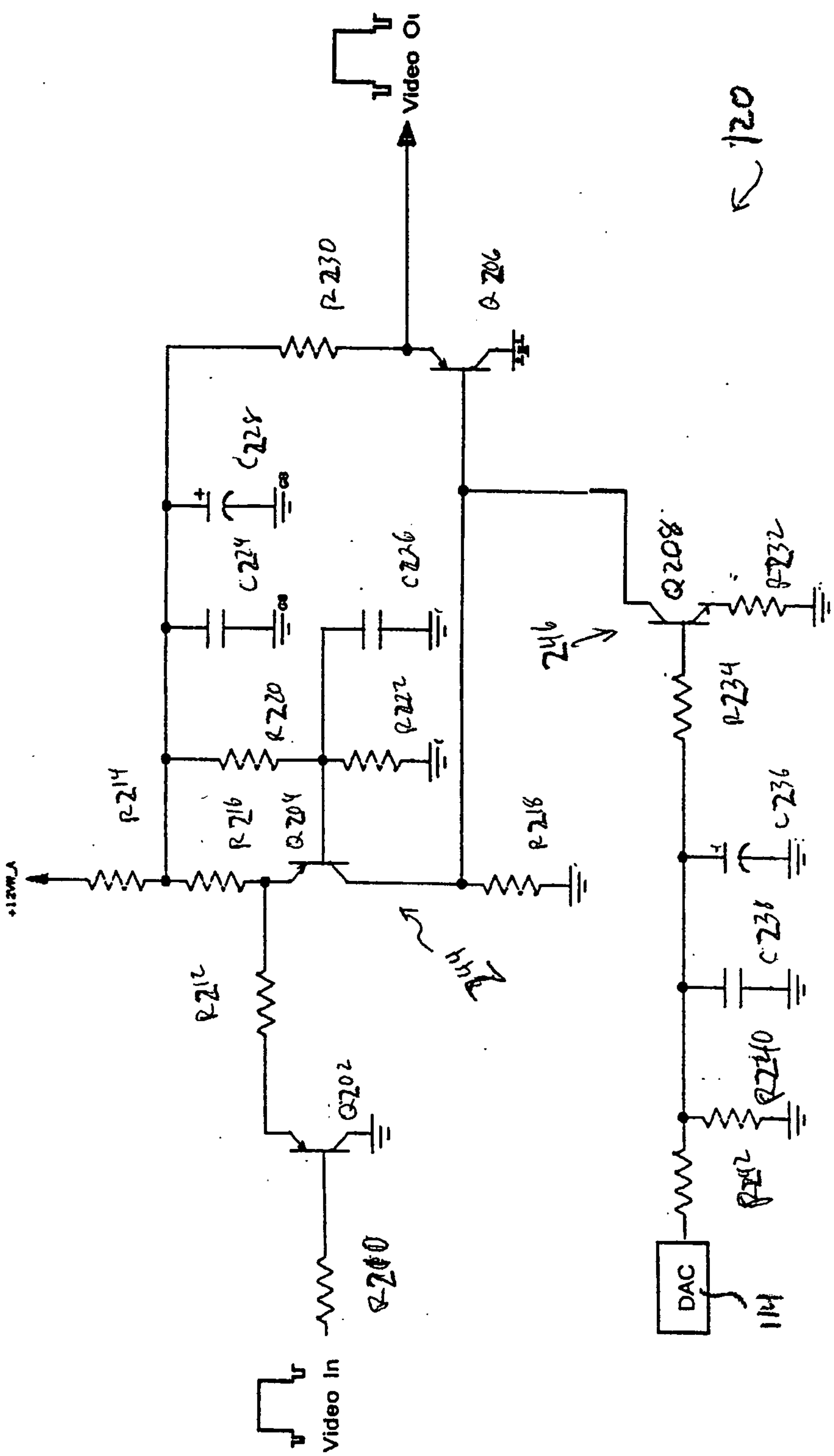
Video In
Video Out
DAC
114
120
244
246
R230
Q206
C225
C224
C226
R220
R222
R214
R216
Q204
R218
R212
Q202
Q208
R232
R234
C236
C238
R240

FIGURE 2

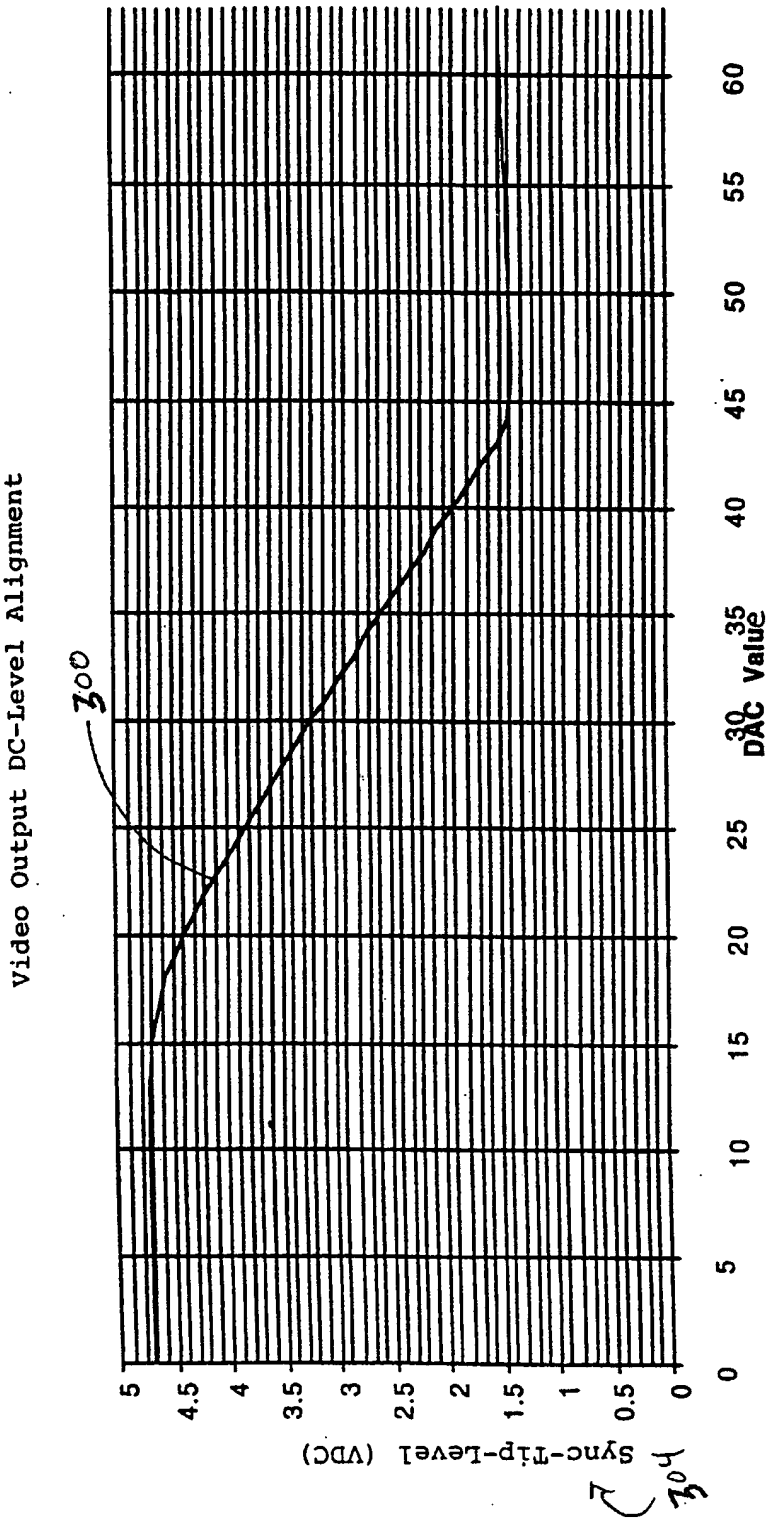

FIGURE 3

INTERNATIONAL SEARCH REPORT

Inter nal Application No
PCT/US 99/22759

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04N5/14 H04N17/04

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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Inter .nal Application No
PCT/US 99/22759

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